WHAT IS CLAIMED IS:

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1. An interconnect for testing a semiconductor component comprising:

a substrate;

a contact on the substrate comprising a recess in the substrate, and a plurality of leads cantilevered over the recess configured to move within the recess to electrically engage a bumped contact on the component, each lead comprising at least one projection for penetrating the bumped contact, and a non-bonding outer layer for preventing bonding of the lead to the bumped contact.

2. The interconnect of claim 1 wherein the leads comprise a deposited and patterned metal layer on the substrate.

3. The interconnect of claim 1 wherein the leads comprise a polymer tape attached to the substrate.

4. The interconnect of claim 1 wherein the leads comprise etched beams on the substrate.

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5. The interconnect of claim 1 wherein the leads have a shape that matches a topography of the bumped contact.

6. An interconnect for testing a semiconductor component comprising:

a substrate;

a recess in the substrate;

a plurality of leads on the substrate cantilevered over the recess and configured to move within the recess to electrically engage a bumped contact on the component, each lead having a cantilever length, a width, a thickness and a

modulus of elasticity selected to provide a desired spring constant; and

a conductive connecting segment proximate to the recess electrically connecting the leads to one another.

7. The interconnect of claim 6 wherein the connecting segment encircles a periphery of the recess.

8. The interconnect of claim 6 further comprising a conductive via in the substrate in electrical communication with the connecting segment.

9. The interconnect of claim 6 wherein each lead comprises an enlarged portion attached to the substrate and a terminal portion for contacting the bumped contact.

10. The interconnect of claim 6 wherein the leads comprise a metal selected from the group consisting of tungsten, titanium, nickel, platinum, iridium, or vanadium.

11. The interconnect of claim 6 the plurality of leads comprise four leads.

12. An interconnect for testing a semiconductor component comprising:

a substrate;

a recess in the substrate;

a plurality of leads on the substrate cantilevered over the recess and configured to move within the recess to electrically engage a bumped contact on the component, the leads having a curved shape which substantially matches a topography of the bumped contact.

13. The interconnect of claim 12 wherein the leads include a conductive connecting portion proximate to the recess for electrically connecting the leads to one another.

14. The interconnect of claim 12 wherein each lead comprises at least one projection for electrically engaging the bumped contact.

15. The interconnect of claim 12 wherein each lead comprises a non-bonding outer layer.

16. The interconnect of claim 12 wherein the bumped contact comprises solder and the leads comprise a non-solder wettable metal.

17. The interconnect of claim 12 wherein each lead has a cantilevered length, a width and a thickness selected to provide a desired spring constant.

18. The interconnect of claim 12 wherein each lead has an enlarged portion attached to the substrate and a terminal portion for contacting the bumped contact.

19. An interconnect for testing a semiconductor component comprising:

a substrate;

a recess in the substrate; and

a contact on the substrate for electrically engaging a bumped contact on the component, the contact comprising a recess and a plurality of conductive beams within the recess, each conductive beam comprising an etched portion of the substrate and an etched projection at least partially covered with conductive layer configured to penetrate the bumped contact, the conductive beams having a cantilever length, a

width, a thickness, and a modulus of elasticity selected to provide a desired spring constant.

20. The interconnect of claim 19 wherein the substrate comprises silicon and the beam comprises an electrically insulating layer formed thereon.

21. The interconnect of claim 19 wherein the conductive layer comprises a metal that is non-bonding with the bumped contacts.

22. The interconnect of claim 19 wherein the bumped contact comprises solder and the conductive layer comprises a non-solder wettable metal.

23. An interconnect for testing a semiconductor component comprising:

a substrate;

a recess in the substrate;

a tape attached to the substrate comprising a polymer substrate and a plurality of leads on the polymer substrate, the leads cantilevered over an opening in the polymer substrate, and over the recess to form a contact for electrically engaging a bumped contact on the component, the leads in electrical communication with a conductive trace on the polymer substrate.

24. The interconnect of claim 23 wherein the tape further comprises an electrical connector in electrical communication with the conductive trace configured for electrical connection to test circuitry.

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25. A system for testing a semiconductor component comprising:

a carrier for retaining the semiconductor component;

an interconnect on the carrier comprising a substrate, a recess in the substrate, and a plurality of leads cantilevered over the recess configured to move within the recess to electrically engage a bumped contact on the component, each lead comprising at least one projection for penetrating the bumped contact, and a non-bonding outer layer for preventing bonding of the lead to the bumped contact; and

test circuitry in electrical communication with the leads for applying test signals to the component.

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26. The system of claim 25 wherein the leads have a curved shape which substantially matches a topography of the bumped contact.

27. The system of claim 25 wherein the component comprises an element selected from the group consisting of semiconductor dice, semiconductor packages and semiconductor wafers.

28. The system of claim 25 wherein the leads comprise a polymer tape attached to the substrate, and an electrical connector configured for connection to the test circuitry.

29. A system for testing a semiconductor component comprising:

a carrier configured to retain the component;

an interconnect on the carrier comprising:

a substrate;

a recess in the substrate; and

a contact on the substrate for electrically engaging a bumped contact on the component, the contact comprising a recess in the substrate and a plurality of conductive beams within the recess, each conductive beam

comprising an etched portion of the substrate and an etched projection at least partially covered with conductive layer configured to penetrate the bumped contact, the conductive beams having a cantilever length, a width, a thickness, and a modulus of elasticity selected to provide a desired spring constant.

30. The system of claim 29 wherein the interconnect further comprises a conductive via in electrical communication with the conductive beams and a terminal contact electrically connectable to test circuitry.

31. A system for testing a semiconductor component comprising:

a wafer prober;

an interconnect mounted to the wafer prober comprising:

a substrate;

a recess in the substrate;

a plurality of leads on the substrate cantilevered over the recess and configured to move within the recess to electrically engage a bumped contact on the component, each lead having a cantilever length, a width, a thickness and a modulus of elasticity selected to provide a desired spring constant;

a conductive connecting segment proximate to the recess electrically connecting the leads to one another; and

test circuitry in electrical communication with the connecting segment.

32. The system of claim 31 wherein the leads have a curved shape that substantially matches a topography of the bumped contact.

33. The system of claim 31 wherein the leads comprise a polymer tape attached to the substrate and comprising an electrical connector configured in electrical communication with the connecting segment and the test circuitry.

34. A method for fabricating an interconnect for testing a semiconductor component comprising:

providing a substrate;

forming a recess in the substrate; and

forming a plurality of leads on the substrate cantilevered over the substrate and configured to electrically engage a bumped contact on the component, each lead having a cantilever length, a width, a thickness and a modulus of elasticity selected to provide a desired spring constant.

35. The method of claim 34 wherein forming the plurality of leads comprises depositing a metal layer on the substrate and then etching the metal layer.

36. The method of claim 34 wherein forming the plurality of leads comprises attaching a polymer tape to the substrate with the leads formed thereon.

37. The method of claim 34 wherein forming the plurality of leads comprises etching beams in the substrate within the recess and covering the beams with conductive layers.

38. The method of claim 34 further comprising forming an insulating layer on the recess.

39. A method for fabricating an interconnect for testing a semiconductor component comprising:

providing a substrate;

forming a metal layer on the substrate;

etching the metal layer to form a plurality of leads; and

etching a recess in the substrate each lead cantilevered over the substrate and movable within the substrate to electrically engage a bumped contact on the component, each lead having a cantilever length, a width, a thickness and a modulus of elasticity selected to provide a desired spring constant.

40. The method of claim 39 further comprising etching a plurality of projections in the metal layer with each lead comprising at least one projection.

41. The method of claim 39 wherein the leads comprise a metal selected from the group consisting of tungsten, titanium, nickel, platinum, iridium, or vanadium.

42. The method of claim 39 further comprising forming an electrically insulating layer within the recess.

43. The method of claim 39 wherein the substrate comprises silicon and etching the recess comprises an anisotropic etch process.

44. A method for fabricating an interconnect for testing a semiconductor component comprising:

providing a substrate;

forming a recess in the substrate;

providing a tape comprising a polymer substrate comprising an opening therein and a plurality of leads on the substrate cantilevered over the opening;

aligning the leads with the recess; and

attaching the tape to the substrate with the leads cantilevered over the recess to form a contact for electrically engaging a bumped contact on the component.

45. The method of claim 44 further comprising providing the tape with an electrical connector configured for electrical connection to test circuitry.

46. A method for fabricating an interconnect for testing a semiconductor component comprising:

providing a substrate;

etching a recess in the substrate sized and shaped to retain a bumped contact on the component;

etching a plurality of beams within the recess configured to move within the recess and to support the bumped contact within the recess;

etching a plurality of projections on the conductive beams configured to penetrate the bumped contact; and

forming a conductive layer on the beams and the projections to form a contact for electrically engaging the bumped contact.

47. The method of claim 46 further comprising controlling the etching of the beams step to form the beams with a cantilever length, a width, and a thickness selected to provide a desired spring constant.

48. The method of claim 46 wherein the substrate comprises silicon and further comprising forming an electrically insulating layer on the beams prior to forming the conductive layer.